PATENT

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In re Application of:

Iu-Meng Tom Ho

Application No.: 10/810,748

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For: Power and Ground Mesh to Remove Capacitive and Inductive Signal Coupling Effects of Routing in Integrated Circuit Device

Examiner: Not Yet Assigned
Art Unit: 2824

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PRELIMINARY AMENDMENT

Examiner:

Prior to examination of this application, Applicant respectfully requests that the Examiner enter the following amendment.

IN THE CLAIMS:

Please add new claims 56-69 as indicated in the complete listing of claims provided below.

1-20. (canceled)

21. (previously presented) An integrated circuit device, comprising:

a substrate;

circuitry disposed on said substrate;

a plurality of signal lines disposed on said substrate to interconnect portions of said circuitry on said substrate;

a power grid disposed on said substrate, the power grid comprising:

a plurality of first lines having a first thickness to supply a first voltage level to said circuitry on said substrate; and

a plurality of second lines to supply a second voltage level to said circuitry on said substrate;

a shield mesh disposed on said substrate, the shield mesh comprising:

a plurality of third lines having a second thickness to supply a third voltage level on said substrate; and

a plurality of fourth lines to supply a fourth voltage level on said substrate;

wherein each of said signal lines is disposed between and adjacent to a respective one of said third lines of said shield mesh and a respective one of said fourth lines of said shield mesh within a layer on said substrate to reduce effects of electronic cross-talk between nearby ones of said signal lines; and

wherein the first thickness is more than the second thickness; and, a first portion of said first lines of said power grid and a first portion of said third lines of said shield mesh are within a first layer on said substrate.

22. (previously presented) An integrated circuit as in claim 21, wherein said first and second voltage levels are ground and power respectively; and, said third and fourth voltage levels are VSS and VDD respectively.

23. (previously presented) An integrated circuit as in claim 21, wherein segment lengths of said third and fourth lines of said shield mesh are substantially smaller than segment lengths of said first and second lines of said power grid.

24. (previously presented) An integrated circuit as in claim 21, wherein said first portion of said first lines and said first portion of said third lines are parallel along a first direction within said first layer on said substrate; a second portion of said first lines and a second portion of said third lines are parallel along a second direction within a second layer on said substrate; and, said first direction is in an angle with said second direction.

25. (previously presented) An integrated circuit as in claim 24, wherein said shield mesh further comprises a plurality of vias interconnecting said first and second portions of said third lines.

26. (previously presented) An integrated circuit device, comprising:
a substrate;

circuitry disposed on said substrate;

a plurality of signal lines disposed on said substrate to interconnect portions of said circuitry on said substrate;

a power grid disposed on said substrate, the power grid comprising:

a plurality of first lines having a first thickness to supply a first voltage level to said circuitry on said substrate; and

a plurality of second lines to supply a second voltage level to said circuitry on said substrate;

a shield mesh disposed on said substrate, the shield mesh comprising:

a plurality of third lines having a second thickness to supply a third voltage level on said substrate; and

a plurality of fourth lines to supply a fourth voltage level on said substrate;

wherein each of said signal lines is disposed between and adjacent to a respective one of said third lines of said shield mesh and a respective one of said fourth lines of said shield mesh within a respective layer on said substrate to reduce effects of electronic cross-talk between nearby ones of said signal lines; and

wherein, perpendicularly across layers of said substrate, each of said signal lines is vertically adjacent to at least one of a parallel one of said third lines of said shield mesh and a parallel one of said fourth lines of said shield mesh but not vertically adjacent to a parallel signal line.

27. (previously presented) An integrated circuit as in claim 26, wherein said first and second voltage levels are ground and power respectively; and, said third and fourth voltage levels are VSS and VDD respectively; and wherein each of said signal lines is vertically and horizontally shielded.

28. (previously presented) An integrated circuit as in claim 26, wherein said shield mesh further comprises:

first vias interconnecting said third lines across layers of said substrate; and,

second vias interconnecting said fourth lines across layers of said substrate.

29. (previously presented) An integrated circuit device, comprising:

a substrate;

circuitry disposed on said substrate;

a plurality of signal lines disposed on said substrate to interconnect portions of said circuitry on said substrate;

a power grid disposed on said substrate, the power grid comprising:

a plurality of first lines to supply a first voltage level to said circuitry on said substrate; and

a plurality of second lines to supply a second voltage level to said circuitry on said substrate;

a shield mesh disposed on said substrate, the shield mesh comprising:

a plurality of third lines to supply a third voltage level to said circuitry on said substrate; and

a plurality of fourth lines to supply a fourth voltage level to said circuitry on said substrate;

wherein each of said signal lines is disposed between and adjacent to a respective one of said third lines of said shield mesh and a respective one of said fourth lines of said shield mesh within a layer on said substrate to reduce effects of electronic cross-talk between nearby parallel ones of said signal lines; and

wherein said third lines and said fourth lines are gridless.

30. (previously presented) An integrated circuit as in claim 29, wherein said shield mesh further comprises:

first vias interconnecting said third lines across layers of said substrate in close proximity without dependency of grid size; and,

second vias interconnecting said fourth lines across layers of said substrate in close proximity without dependency of grid size.

31. (previously presented) An integrated circuit as in claim 30, wherein said first and second vias are of varying sizes.

32. (previously presented) An integrated circuit as in claim 29, wherein said shield mesh has varying segment sizes that are not bound by grid width.

33. (previously presented) An integrated circuit as in claim 29, wherein said first lines and said second lines have a first thickness; and, said third lines, said fourth lines and said signal lines have a second thickness.

34. (previously presented) An integrated circuit device, comprising:

a substrate;

circuitry disposed on said substrate;

a plurality of signal lines disposed on said substrate to interconnect portions of said circuitry on said substrate;

a shield mesh disposed on said substrate, the shield mesh comprising:

a plurality of first lines to supply a first reference voltage level on said substrate; and

a plurality of second lines to supply a second reference voltage level on said substrate;

two vias both connecting a first one of said signal lines to a second one of said signal lines, said first one and said second one of said signal lines being within a first layer and a second layer on said substrate respectively, said first one and said second one of said signal lines running in an angle;

wherein each of said signal lines is disposed between and adjacent to a respective one of said first lines of said shield mesh and a respective one of said second lines of said shield mesh within a layer on said substrate to reduce effects of electronic cross-talk between nearby ones of said signal lines.

35. (previously presented) An integrated circuit as in claim 34, wherein said first one of said signal lines runs in a first direction in said first layer; said second one of said signal lines runs in a second direction in said second layer; and, said first and second directions are 90 degrees apart.

36. (previously presented) An integrated circuit as in claim 34, wherein said two vias are adjacent each other.

37. (previously presented) An integrated circuit as in claim 34, wherein said first lines and said second lines have a same first thickness.

38. (previously presented) An integrated circuit as in claim 37, wherein said first and second reference voltage levels are ground and power respectively.

39. (previously presented) An integrated circuit device as in claim 37, further comprising:

a power grid disposed on said substrate, the power grid comprising:

a plurality of third lines having a second thickness to supply a third voltage level to said circuitry on said substrate; and

a plurality of fourth lines to supply a fourth voltage level to said circuitry on said substrate;

wherein said second thickness is substantially larger than said first thickness.

40. (previously presented) An integrated circuit as in claim 39, wherein said fourth lines have said second thickness.

41. (previously presented) An integrated circuit as in claim 40, wherein said first and second reference voltage levels are VSS and VDD respectively; and, said third and fourth voltage levels are ground and power respectively.

42. (previously presented) An integrated circuit device as in claim 39, wherein said shield mesh further comprises:

a plurality of first vias in close proximity interconnecting said first lines of said shield mesh across layers of said substrate; and,

a plurality of second vias in close proximity interconnecting said second lines of said shield mesh across layers of said substrate.

43. (previously presented) A method of designing an integrated circuit (IC), said method comprising:

creating a representation of a shielding mesh in at least one layer of said IC, said shielding mesh having a first plurality of lines which are designed to provide a first reference voltage and having a second plurality of lines which are designed to provide a second reference voltage;

creating a representation of a power grid in said at least one layer of said IC, said power grid having a plurality of first reference voltage lines and a plurality of second reference voltage lines, said power grid for supplying power to circuitry in said IC, and wherein said plurality of first and second reference voltage lines have either: (a) an average line spacing which is substantially larger than an average line spacing in said shielding mesh, or (b) a thickness which is larger than lines in said shielding mesh.

44. (previously presented) A method as in claim 43, wherein the method is performed at least in part by an EDA tool.

45. (previously presented) A method as in claim 44, wherein said method uses initial code written in an HDL.

46. (previously presented) A method as in claim 44, further comprising:

creating a representation of a plurality of signal lines routed through said shielding mesh.

47. (previously presented) A method of designing an integrated circuit (IC), said method comprising:

creating a representation of a shielding mesh in at least a first and second layers of said IC, said shielding mesh having a first plurality of lines which are designed to provide a first reference voltage and having a second plurality of lines which are designed to provide a second reference voltage;

creating a representation of a plurality of signal lines in said shielding mesh, wherein perpendicularly across layers of said IC, each of said signal lines is vertically adjacent to at least one of a parallel one of said first plurality of lines and a parallel one of said second plurality of lines but not vertically adjacent to a parallel signal line.

48. (previously presented) A method as in claim 47, wherein the method is performed at least in part by an EDA tool.

49. (previously presented) A method as in claim 47, wherein said method uses initial code written in an HDL.

50. (previously presented) A method of designing an integrated circuit (IC), said method comprising:

creating a representation of a shielding mesh in at least one layer of said IC, said shielding mesh having a first plurality of lines which are designed to provide a first reference voltage and having a second plurality of lines which are designed to provide a second reference voltage;

creating a representation of a plurality of signal lines routed through said shielding mesh, wherein said shielding mesh is gridless.

51. (previously presented) A method as in claim 50, wherein the method is performed at least in part by an EDA tool.

52. (previously presented) A method as in claim 51, wherein said method uses initial code written in an HDL.

53. (previously presented) A method of designing an integrated circuit (IC), said method comprising:

creating a representation of a shielding mesh in at least one layer of said IC, said shielding mesh having a first plurality of lines which are designed to provide a first reference voltage and having a second plurality of lines which are designed to provide a second reference voltage; and

creating a representation of a plurality of signal lines routed through said shielding mesh, wherein at least one of said signal lines is coupled to a signal line on another layer through at least two vias.

54. (previously presented) A method as in claim 53, wherein the method is performed at least in part by an EDA tool.

55. (previously presented) A method as in claim 54, wherein said method uses initial code written in an HDL.

56. (new) An integrated circuit (IC), comprising:

a shielding mesh having a first layer and a second layer, the first layer having a first conductor, the second layer having a second conductor; and

two vias each connecting from the first conductor of the first layer to the second conductor of the second layer.

57. (new) The integrated circuit of claim 56, wherein the first conductor and the second conductor are not parallel.

58. (new) The integrated circuit of claim 56, wherein the first conductor and the second conductor are in close proximity.

59. (new) The integrated circuit of claim 58, wherein a distance between the first conductor and the second conductor is smaller than an average spacing between parallel lines of the shielding mesh.

60. (new) A method of designing an integrated circuit (IC), the method comprising:

generating a representation of a shielding mesh having a first layer and a second layer, the first layer including a first conductor, the second layer including a second conductor; and

generating a representation of two vias, each of the two vias connecting from the first conductor to the second conductor.

61. (new) The method of claim 60, wherein the first conductor and the second conductor are not parallel.

62. (new) The method of claim 60, wherein the first conductor and the second conductor are in close proximity.

63. (new) The method of claim 62, wherein the method is performed at least in part by an EDA tool.

64. (new) A machine readable medium containing executable computer program instructions which when executed by a digital processing system cause said system to perform a method of designing an integrated circuit (IC), the method comprising:

generating a representation of a shielding mesh having a first layer and a second layer, the first layer including a first conductor, the second layer including a second conductor; and

generating a representation of two vias, each of the two vias connecting from the first conductor to the second conductor.

65. (new) The medium of claim 64, wherein the first conductor and the second conductor are not parallel.

66. (new) The medium of claim 64, wherein the first conductor and the second conductor are in close proximity.

67. (new) A data processing system for designing an integrated circuit (IC), the system comprising:

means for generating a representation of a shielding mesh having a first layer and a second layer, the first layer including a first conductor, the second layer including a second conductor; and

means for generating a representation of two vias, each of the two vias connecting from the first conductor to the second conductor.

68. (new) The system of claim 67, wherein the first conductor and the second conductor are not parallel.

69. (new) The system of claim 68, wherein the first conductor and the second conductor are in close proximity.

REMARKS

This preliminary amendment adds additional claims which are supported by at least Figure 7 and the specification on page 15; thus, no new matter has been added.

Please charge any shortages or credit any overages to Deposit Account No. 02-2666. Furthermore, if an extension is required, Applicant hereby requests such extension.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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